

Application No. 09/892,291  
Response to OA of 08/30/04

**Amendments to the Claims**

**This listing of claims will replace all prior versions, and listings, of the claims:**

1. (currently amended) A method for chip testing, comprising the steps of:
  - establishing a communications link between a chip and a computer tester;
  - receiving on the chip an initial test algorithm over a communications link;
  - testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;
  - collecting a set of failure information in response to the testing; ~~and~~
  - transmitting the failure information from the chip to the computer over the communications link; and
  - minimizing data transmitted from the chip to the computer by comparing failed data patterns in a buffer on the chip with previous failed data patterns.
2. (original) The method of claim 1, wherein:
  - the receiving step includes the step of receiving a second test algorithm whose coverage differs from the initial test algorithm; and
  - the testing step includes the step of testing the chip in accordance with the second test algorithm.
3. (original) The method of claim 1, wherein the testing step includes the step of:
  - testing a memory array within the chip in accordance with the algorithm.
4. (original) The method of claim 3 further comprising the step of:
  - generating a bit-map on the computer, from the failure information, of failed bit locations within the memory array.
5. (original) The method of claim 3 wherein the collecting step includes the step of:
  - collecting a set of failed address information in response to the testing.
6. (original) The method of claim 5 wherein:

Application No. 09/892,291  
Response to OA of 08/30/04

the testing step includes the steps of,  
writing a set of data to an address under test in the memory array  
reading out data from the address; and  
the collecting step includes the step of adding the address under test to the set of  
failed address information, if the written set of data is not equivalent to the set of data  
read-out.

7. (original) The method of claim 6 wherein the collecting step includes the step of:  
adding bit locations in the address under test, in which the written set of data  
differs from the set of data read-out, to the set of failed address information.

8. (original) The method of claim 1, further including the step of:  
repairing the chip using redundancy allocation techniques based on the set of  
failure information.

9. (original) The method of claim 1 further comprising the steps of:  
identifying a number of circuit redundancies within the chip; and  
halting testing if the failure information exceeds the number of redundancies.

10. (canceled)

11. (canceled)

12. (currently amended) A method for chip testing, comprising the steps of:  
establishing a communications link between a chip and a computer tester;  
receiving on the chip an initial test algorithm over a communications link;  
testing a memory array within the chip, using a built-in self-test circuit (BIST) on  
the chip, in accordance with the initial test algorithm;  
adding an address under test and those bit locations which failed to a set of failed  
address information, if a set of data written to the address under test is not equivalent to a  
set of data read-out from the address under test;

Application No. 09/892,291  
Response to OA of 08/30/04

transmitting the failed address information from the chip to the computer over the communications link; ~~and~~

minimizing data transmitted from the chip to the computer by comparing failed data patterns in a buffer on the chip with previous failed data patterns; and

generating a bit-map on the computer, from the failed address information, of the failed bit locations within the memory array.

13. (currently amended) A computer-usable medium embodying computer program code for commanding a computer to perform chip testing comprising the steps of:

establishing a communications link between a chip and a computer tester;

receiving on the chip an initial test algorithm over a communications link;

testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;

collecting a set of failure information in response to the testing; ~~and~~

transmitting the failure information from the chip to the computer over the communications link; and

minimizing data transmitted from the chip to the computer by comparing failed data patterns in a buffer on the chip with previous failed data patterns.

14. (original) The medium of claim 13, wherein the testing step includes the step of:

testing a memory array within the chip in accordance with the algorithm.

15. (original) The medium of claim 14 further comprising the step of:

generating a bit-map on the computer, from the failure information, of failed bit locations within the memory array.

16. (original) The medium of claim 14 wherein the collecting step includes the step of:

collecting a set of failed address information in response to the testing.

17. (original) The medium of claim 16 wherein:

the testing step includes the steps of,

Application No. 09/892,291  
Response to OA of 08/30/04

writing a set of data to an address under test in the memory array  
reading out data from the address; and

the collecting step includes the step of adding the address under test to the set of failed address information, if the written set of data is not equivalent to the set of data read-out.

18. (original) The medium of claim 17 wherein the collecting step includes the step of:  
adding bit locations in the address under test, in which the written set of data differs from the set of data read-out, to the set of failed address information.

19. (original) The medium of claim 13, further including the step of:  
repairing the chip using redundancy allocation techniques based on the set of failure information.

20. (currently amended) A system for chip testing comprising a:  
means for establishing a communications link between a chip and a computer tester;  
means for receiving on the chip an initial algorithm over a communications link;  
means for testing the chip, using a built-in self-test circuit (BIST) on the chip, in accordance with the initial test algorithm;  
means for collecting a set of failure information in response to the testing; and  
means for transmitting the failure information from the chip to the computer over the communications link; and  
means for minimizing data transmitted from the chip to the computer by comparing failed data patterns in a buffer on the chip with previous failed data patterns.

21. (currently amended) A system for chip testing, comprising:  
a communications link;  
a computer, operating a set of chip testing software; and  
a chip under test coupled to the computer by the communications link, having,  
a memory array; and

Application No. 09/892,291  
Response to OA of 08/30/04

a Built In Self Test (BIST) module for testing the memory array in response to test algorithms received from the computer and transmitting those addresses within the memory array which failed testing, wherein the BIST module further minimizes data transmitted to the computer by comparing failed data patterns in a buffer on the chip with previous failed data patterns.

22. (original) The system of claim 21, wherein the chip includes:

redundant circuits responsive to repair programs activated on the computer in response to the address failures detected during testing.

23. (previously presented) The method of claim 1 wherein collecting a set of failure information further comprises temporarily storing the failure information to a buffer on the chip.

24. (previously presented) The method of claim 1 wherein transmitting the failure information further comprises transmitting the failure information from a communication module on the chip to the computer over the communication link.

25. (canceled)

26. (previously presented) The method of claim 1 wherein the chip and computer exchange messages over a serial bus protocol.

27. (previously presented) The method of claim 1 wherein the computer tester is a personal computer.

28. (previously presented) The medium of claim 13 wherein collecting a set of failure information further comprises temporarily storing the failure information to a buffer on the chip.

Application No. 09/892,291  
Response to OA of 08/30/04

29. (previously presented) The medium of claim 13 wherein transmitting the failure information further comprises transmitting the failure information from a communication module on the chip to the computer over the communication link.

30. (canceled)

31. (previously presented) The system of claim 20 wherein the means for collecting a set of failure information further comprises temporarily storing the failure information to a buffer on the chip.

32. (previously presented) The system of claim 20 wherein the means for transmitting the failure information further comprises transmitting the failure information from a communication module on the chip to the computer over the communication link.

33. (canceled)

34. (previously presented) The system of claim 21 wherein the computer is a personal computer.

35. (previously presented) The system of claim 21 wherein the computer receives, via the communication link, the addresses that failed testing and, upon receipt of the failed addresses, reconstructs a bit-map that identifies the failed addresses.

36. (previously presented) The system of claim 35 wherein the computer executes a redundancy allocation algorithm that generates a fuse map for repairing the failed addresses.

37. (canceled)